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April 7, 2000

Attorney Docket No.: 07402-039001

Box Patent Application
Assistant Commissioner for Patents
Washington, DC 20231

Presented for filing is a new patent application claiming priority from a provisional patent application of:

Applicant: LARS S. CARLSON AND SHULAI ZHAO

Title: INSULATOR/METAL BONDING ISLAND FOR ACTIVE AREA SILVER EPOXY BONDING

Enclosed are the following papers, including those required to receive a filing date under 37 CFR 1.53(b):

	Pages
Specification	10
Claims	4
Abstract	1
Declaration	2
Drawing(s)	4

Enclosures:

— Small entity statement. This application is entitled to small entity status.
— Information Disclosure Statement
— Form PTO-1449
— Postcard.

CERTIFICATE OF MAILING BY EXPRESS MAIL

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April 7, 2000
Date of Deposit

Derek Norwood
Signature

Derek W. Norwood
Typed or Printed Name of Person Signing Certificate

Under 35 USC §119(e)(1), this application claims the benefit of prior U.S. provisional application 60/128,626, filed April 9, 1999.

There are 17 claims, 3 are independent.

Basic filing fee	$345
Total claims in excess of 20 times $9	$0
Independent claims in excess of 3 times $39	$0
Fee for multiple dependent claims	$0
Total filing fee:	$345

A check for the filing fee is enclosed. Please apply any other required fees or credits to deposit account 06-1050, referencing the attorney document number shown above.

If this application is found to be incomplete, or if a telephone conference would otherwise be helpful, please call the undersigned at (858) 678-5070.

Kindly acknowledge receipt of this application by returning the enclosed postcard.

Please send all correspondence to:

JAMES T. HAGLER
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Respectfully submitted,

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for James T. Hagler
Reg. No. 40,631
Enclosures
JTH/keh
10028131.doc

ATTORNEY DOCKET NO. 07402-039001

Applicant or Patentee: Carlson, et al.
Serial or Patent No.:
Filed or Issued: April 7, 2000
For: INSULATOR/METAL BONDING ISLAND FOR ACTIVE AREA SILVER EPOXY BONDING

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) and 1.27(c)) — SMALL BUSINESS CONCERN

I hereby declare that I am

[] the owner of the small business concern identified below:
[X] an official of the small business concern empowered to act on behalf of the concern identified below:

Name of Small Business Concern: DIGIRAD CORPORATION
Address of Small Business Concern: 9350 Trade Place
San Diego, CA 92126-6334

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled INSULATOR/METAL BONDING ISLAND FOR ACTIVE AREA SILVER EPOXY BONDING by inventor(s) LARS S. CARLSON AND SHULAI ZHAO described in:

[X] the specification filed herewith.
[] application serial no. _, filed _.
[] patent no. _, issued _.

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e). *NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

Full Name: _____
Address: _____

[] INDIVIDUAL [] SMALL BUSINESS CONCERN [] NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status when any new rule 53 application is filed or prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent on which this verified statement is directed.

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Signature: _____ **Date:** 4-7-00

Attorney's Docket No.: 07402-039001

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: INSULATOR/METAL BONDING ISLAND FOR ACTIVE AREA SILVER EPOXY BONDING

APPLICANT: LARS S. CARLSON AND SHULAI ZHAO

CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No. EL584743128US

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April 7, 2000
Date of Deposit

Signature

Derek W. Norwood
Typed or Printed Name of Person Signing Certificate

INSULATOR/METAL BONDING ISLAND FOR ACTIVE-AREA SILVER EPOXY BONDING

CROSS-REFERNCE TO RELATED APPLICATION

This application claims benefit of the priority of U.S. Provisional Application Serial Number 60/128,626, filed April 9, 1999 and entitled "An Oxide/Metal Bonding Island for Active Area Silver Conductive Epoxy Bonding."

BACKGROUND

This invention relates to semiconductor detectors, and more particularly to the improvement of the electrical and mechanical integrity of such detectors connected to external structures or electronics.

In a conventional flip-chip 100 shown in FIG. 1, a semiconductor chip or die can have bumped terminations spaced around an active area of the die. The terminations are intended for face-to-face attachment of the semiconductor die to a substrate 102 or another semiconductor die. The bumped terminations of the flip-chip 100 often include an array of minute solder balls or epoxy bonds 104 disposed on a front attachment surface of a semiconductor die. The attachment of a flip-chip 100 to a substrate 102 or another semiconductor involves aligning the epoxy bonds 104 on the flip- chip 100 with a plurality of contact points 106 on a facing surface 108 of the substrate 102. The contact points 106 are configured to be a mirror image of the epoxy bond arrangement 104 on the flip-chip 100. A plurality of epoxy bonds 104 may also be formed on the facing surface of the substrate 102 at the contact points 106. In some applications, semiconductor illumination detector chips are

attached to structures such as printed circuit boards (PCBs) or signal processing electronics in a flip-chip interconnection.

Several techniques exist for forming flip-chip interconnections between semiconductor photodetectors and external structures. These include solder bump interconnection, silver epoxy bonding, and indium bump bonding. The silver epoxy bonding is a relatively simple technique that has been widely used for flip-chip bonding of semiconductor photodetectors to external structures. The silver epoxy is silver-filled epoxy having a suspension of silver particles in an epoxy paste. The paste, mixed with a compatible hardening agent, is applied in liquid form to the contacts on the photodetector and/or the external structures. The front surfaces of the chip and external structure are aligned mechanically. The surfaces are then brought into sufficiently close proximity so that the silver epoxy forms a bridge between the mating contacts on the two components. However, the liquid nature of the epoxy itself imposes limits on the minimum spacing between adjacent contacts that can be bonded. An appropriate curing cycle causes the silver epoxy to cure into conductive, rigid or semi-rigid, interconnections between the two components.

Since the metal electrical contacts on a photodetector often resides directly on the surface of the semiconductor material itself, any migration of the components of the silver epoxy through the metal contact can cause degradation of the electrical properties of photodetector structures. Further, an exposure of the flip-chip photodetector to repeated cycles between low and high temperatures may cause failure of the electrical and mechanical connection. Such failures are often caused by mechanical stresses to the assembly resulting from the difference between the coefficients of thermal expansion (CTE) of the semiconductor material and the external structure. Forces applied to the assembly by other

means may also cause failure of the interconnection. In some cases, the stresses on the metal-to-semiconductor interface are sufficient to pull a portion of the semiconductor material away from the surface of the chip.

SUMMARY

The present disclosure includes a semiconductor interconnection device having a semiconductor die, a plurality of epoxy bonds, and an array of insulating islands. The semiconductor die has a plurality of conductive contacts. The plurality of epoxy bonds contains a metallic component such as silver. The epoxy bonds are configured to provide interconnection between the semiconductor die and an external structure. The plurality of epoxy bonds is selectively applied to the plurality of conductive contacts on the semiconductor die and corresponding conductive contacts on the external structure. The array of insulating islands is coupled to the plurality of conductive contacts. The islands are configured to prevent migration of the metallic substance from the plurality of epoxy bonds to the semiconductor die through the plurality of conductive contacts.

The present disclosure also includes a method of manufacturing a flip-chip interconnection device. The method includes providing an array of insulating islands on a semiconductor die, applying a plurality of metal contacts over the array of insulating islands, and selectively depositing an array of epoxy bonds on the plurality of metal contacts. The array of insulating islands prevents migration of metallic component in the array of epoxy bonds into the semiconductor die.

The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

FIG. 1 is a top perspective view showing a flip-chip interconnection with an external structure substrate.

FIG. 2 is a cross-section of a conventional p-i-n photodiode connected to an external structure by means of a silver epoxy bond.

Fig. 3 is a cross-section of a p-i-n photodiode in accordance with one embodiment of the present invention.

FIG. 4 is a flowchart of a flip-chip interconnection device manufacturing process in accordance with an embodiment of the present invention

Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

In recognition of the above, a new system has been developed to provide flip-chip connection with reduced degradation of the electrical and mechanical properties. The

inventors recognized that in forming a flip-chip interconnection using silver epoxy bonding, the degradation of the electrical properties of metal-semiconductor structures was caused by silver migration into the active area. This recognition is supported by A. Castaldini, Degradation Effects at Aluminum-Silicon Schottky Diodes, Electrochemical and Solid-State Letters, Vol. 1, No. 2, pp. 83-85 (1998).

A simplified cross-section of a conventional semiconductor detector, such as a photovoltaic detector or a photoconductive detector, is shown in FIG. 2. The photovoltaic detector can include a p-n junction photosensor, a p-i-n diode photodetector, or a metal-semiconductor (Schottky) photosensor. As an example, FIG. 2 is described in terms of a p-i-n diode photodetector or a p-i-n photodiode 200. The p-i-n photodiode 200 is formed on a semiconductor substrate 202, and is connected to a mating contact 218 on a substrate 205 of an external structure 204. Near the top surface of the lightly doped n-type semiconductor substrate 202, a heavily doped p-type region 206 has been fabricated. The lightly doped n-type semiconductor is often denoted as intrinsic or i-type. A heavily doped n-type layer and an appropriate contact (not shown) complete the p-i-n structure.

In conventional silicon (Si) technology, a thermally-grown silicon dioxide field oxide 210 is formed over a face surface 212 of a semiconductor wafer 202 to passivate the Si surface. The oxide thus acts as a passivation film 210. The passivation film 210 is selectively etched to expose the conductive electrode 206 formed with the heavily doped p-type region. A metal contact 208 is then applied over the face surface 214 of the passivation film 210. The conductive electrode 206 formed with the heavily doped p-type region facilitates formation of an ohmic connection to the metal contact 208. For photodiodes fabricated in other materials, suitable insulators may be grown or deposited for passivation.

A silver epoxy bond 216 connects the metal contact 208 to the mating contact 218 on the substrate 205 of the external structure 204. Silver migration through the metal contact 208 at several locations 220 is shown. The silver migration at these locations 220 leads to the formation of silver-contaminated regions 222 at and/or below the semiconductor surface. These regions 222 degrade the electrical properties of the semiconductor device such as a photodetector.

FIG. 3 shows a new semiconductor illumination detector, such as a p-i-n photodiode 300, in accordance with one embodiment of the present system. The present p-i-n photodiode 300 promotes prevention of degradation by silver migration.

In the photodiode structure 300 of FIG. 3, an insulating island 324 is formed on the surface 326 of the heavily doped p-type conductive electrode 306 prior to deposition of the metal contact 308. Once the metal contact 308 is applied over the face surface 314 of the passivation film 310, the silver epoxy bond 316 connects the metal contact 308 to the mating contact 318 on the substrate 305 of the external structure 304. Again, the silver migration through the metal contact 308 occurs at several points 320. However, in contrast to the situation depicted in FIG. 2, the insulating island 324 acts as a barrier to silver migration. The insulating island 324 prevents the formation of contaminated regions such as those represented by 222 in FIG. 2. Therefore, degradation of the photodiode 300 by silver contamination is substantially reduced.

In one embodiment, the insulating island 324 comprises a layer of insulating material. In another embodiment, the insulating island 324 is thermally grown silicon dioxide.

The portion of the metal contact 308 directly over the insulating island 324 is referred to as an insulator/metal bonding structure 330. This insulator/metal bonding structure 330

provides a direct contact between the silver epoxy bond 314 and the semiconductor material 306, thereby providing the required electrical connection between the photodiode 300 and the external structure 320.

The insulating island 324 also provides a mechanical buffer region to mitigate the transmission of stress from the silver epoxy bond into the semiconductor. The most common stress is due to the inherently large coefficient of thermal expansion (CTE) mismatch between the semiconductor substrate and the substrate of the external structure. The electronic packages are subject to two types of heat exposures: process cycles, which are often high in temperature but few in number; and operation cycles, which are numerous but less extreme. If either the flip chips or substrates are unable to repeatedly bear their share of the system thermal mismatch, on or more elements of the electronic package will fracture, which destroys the functionality of the electronic package.

As an electronic package dissipates heat to its surroundings during operation, or as the ambient system temperature changes, differential thermal expansions cause stresses to be generated in the interconnection structures between the semiconductor die and the substrate. These stresses produce instantaneous elastic and, most often, plastic strain, as well as time-dependent strains in the joint, especially within its weakest segment. Thus, the CTE mismatch between chip and substrate will cause a shear displacement to be applied on each terminal which can fracture the connection.

FIG. 4 is a flowchart of a flip-chip interconnection device manufacturing process in accordance with an embodiment of the present invention. At step 400, an array of insulating islands is provided on a semiconductor die. A plurality of metal contacts is applied over the array of insulating islands at step 402. An array of epoxy bonds is selectively deposited on

the plurality of metal contacts at step 404. At step 406, the array of epoxy bonds is aligned on top of respective metal contacts on an external structure. Finally, the semiconductor die is bonded to the external structure at step 408.

Insulator/metal bonding islands 324, 330, as described in connection with FIG. 3, have been embodied in silicon p-i-n photodiode arrays with sixteen individual photodiode pixels in a 4x4 array. These arrays were fabricated in high resistivity (> 1000ohm-cm) silicon substrates using conventional silicon process technology. Active p-type contacts to these devices were approximately 2.9 x 2.9 mm^2. Circular, thermally grown silicon dioxide bonding islands approximately 630 micrometers in diameter and nominally 0.25 micrometers thick were fabricated at one or more locations over each active p-type contact. A thermally-grown silicon dioxide field oxide, nominally 1 micrometer thick, passivated the gaps between the pixels and over other regions of the chips. Metal contacts were formed by sputter deposition of approximately 1 micrometer of aluminum containing nominally 1% of dissolved silicon (Al:1%Si) over nearly the entire active p-type region and overlapping the edges of the field oxide. In some embodiments, a double-layer metal system, having Al:1%Cu over Al:1%Si, with each layer nominally 1 micrometer thick was used. The second metal layer was connected to the first layer through holes etched in a second-level passivation insulator and deposited over the field oxide. Both silicon dioxide and silicon nitride have been used for this second-level passivation. The single and double-layer metal systems have been used in conjunction with an under bump metallization (UBM) system. The UBM is used to facilitate fabrication of solder balls on the chips. The UBM used in the embodiment is fabricated on top of the metal contacts by addition of 5 to 7 micrometers of

nickel deposited by electroless plating, followed by approximately 0.2 micrometers of electroless gold.

All of the metal systems were subject to silver migration. Both of the layers in this type of UBM were porous, and fabrication of these layers frequently left gaps between the UBM and the walls of the second layer glass through which silver could migrate.

Several versions of the photodiode arrays have been produced with each chip requiring 18 to 20 silver-epoxy bonds to printed circuit boards (PCBs). The PCBs carried external signal processing electronics. Silver epoxy has been used for direct chip-to-PCB bonds and also in hybrid silver epoxy/solder bump bonds. Thousands of chips have been bonded to PCBs by one or both of these methods, and chip/PCB assemblies fabricated by these methods have been embodied into prototype and production versions of the DIGIRAD 2020*tc*™, a commercial solid-state gamma-ray imager.

Even under accelerated life tests, almost no performance degradation attributable to silver migration was observed. Although any contamination of the semiconductor material by silver migration would degrade the leakage currents of these devices, the test results showed that the photodiode arrays have extremely low reverse-bias leakage currents less than 1nA/cm^2. It is important to note that these devices are uniquely sensitive to contamination because they have such low leakage currents.

A number of embodiments of the invention have been described above for illustrative purposes. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. For example, the term p-i-n is used in the above description to represent collectively p-i-n and p-n structures and their complementary n-p and n-i-p devices. All statements and claims with respect to specific

semiconductor structures are for illustrative purposes only. They apply qualitatively to the complementary structure in which all of the following can be simultaneously replaced with their (polarity-reversed) complement: conductivity types, charge carriers, electrical potentials and electric fields. Accordingly, other embodiments are within the scope of the following claims.

WHAT IS CLAIMED IS:

1. A semiconductor interconnection system, comprising:

a semiconductor die;

first and second conductive contacts, said first conductive contact coupled to a surface of said semiconductor die, and said second conductive contact coupled to an external structure or die;

a silver epoxy bond interposed between said first and second conductive contacts, said epoxy bond providing electrical and mechanical interconnection between said semiconductor die and said external structure; and

an insulating island configured to prevent migration of silver from said silver epoxy bond to said semiconductor die through said first conductive contact.

2. The system of claim 1, wherein said semiconductor die is a photodetector.

3. The system of claim 2, wherein said photodetector is a p-i-n photodiode.

4. The system of claim 1, wherein said insulating island comprises a layer of oxide.

5. The system of claim 1, further comprising:

a conductive electrode heavily doped with p-type material at the surface of said semiconductor die to provide electrical connection between said semiconductor die and said external structure.

6. The system of claim 5, further comprising an insulator/metal bonding structure disposed above said insulating island, said insulator/metal bonding island providing direct contact between the silver epoxy bond and the conductive electrode, thereby providing required electrical connection between said semiconductor die and said external structure.

7. The system of claim 1, wherein said semiconductor die is silicon and the insulating island is thermally grown silicon dioxide.

8. The system of claim 1, wherein said insulating island provides reduction in transmission of mechanical stress from said silver epoxy bond into the semiconductor die.

9. A semiconductor flip-chip, comprising:

a semiconductor die having a plurality of conductive contacts;

a plurality of epoxy bonds having a metallic component, said epoxy bonds configured to provide interconnection between said semiconductor die and an external structure, said plurality of epoxy bonds selectively applied to said plurality of conductive contacts on said semiconductor die and corresponding conductive contacts on the external structure; and

an array of insulating islands coupled to said plurality of conductive contacts, said insulating islands configured to prevent migration of said metallic substance from said plurality of epoxy bonds to said semiconductor die through said plurality of conductive contacts.

10. The flip-chip of claim 9, wherein said metallic substance is silver.

11. The flip-chip of claim 9, wherein said semiconductor die is a semiconductor illumination detector chip.

12. The flip-chip of claim 9, wherein said plurality of conductive contacts on said semiconductor die forms connections to an array of photodiode pixels.

13. The flip-chip of claim 11, wherein said array of insulating islands prevents degradation of low reverse-bias leakage currents in said array of photodiode pixels.

14. A method of manufacturing a flip-chip interconnection device, comprising:

providing an array of insulating islands on a semiconductor die;

applying a plurality of metal contacts over said array of insulating islands; and

selectively depositing an array of epoxy bonds on said plurality of metal contacts, where said providing said array of insulating islands prevents migration of metallic substance in said array of epoxy bonds into said semiconductor die.

15. The method of claim 14, further comprising:

aligning said array of epoxy bonds on top of respective metal contacts on an external structure; and

bonding said semiconductor die to said external structure.

16. The method of claim 14, wherein said providing said array of insulating islands includes depositing a layer of thermally grown silicon dioxide.

17. The method of claim 14, wherein said applying said plurality of metal contacts provides an array of insulator/metal bonding islands disposed on top of said array of insulating islands, said array of insulator/metal bonding islands operating to provide direct electrical contact between the array of epoxy bonds and the semiconductor die.

ABSTRACT

A semiconductor interconnection device having a semiconductor die, a plurality of epoxy bonds, and an array of insulating islands is disclosed. The semiconductor die has a plurality of conductive contacts. The plurality of epoxy bonds has a metallic substance such as silver. The epoxy bonds are configured to provide interconnection between the semiconductor die and an external structure. The plurality of epoxy bonds is selectively applied to the plurality of conductive contacts on the semiconductor die and corresponding conductive contacts on the external structure. The array of insulating islands is coupled to the plurality of conductive contacts. The islands are configured to prevent migration of the metallic substance from the plurality of epoxy bonds to the semiconductor die through the plurality of conductive contacts.

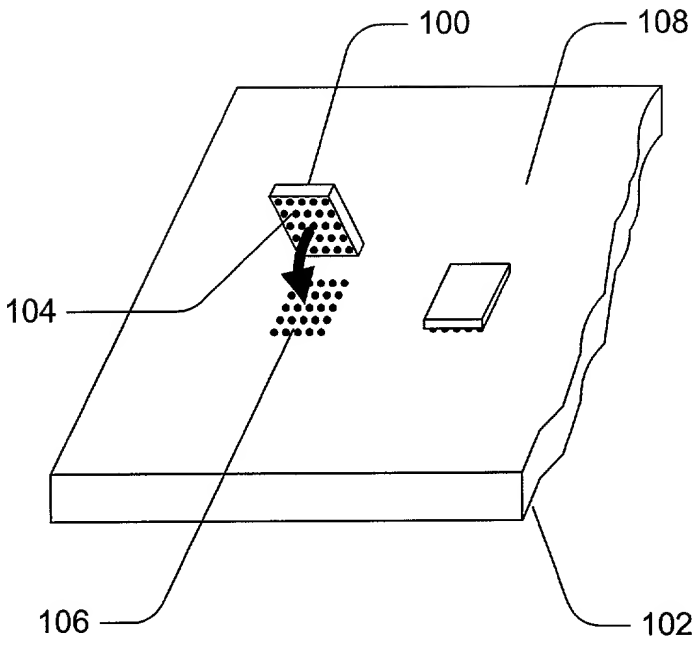

FIG. 1
(PRIOR ART)

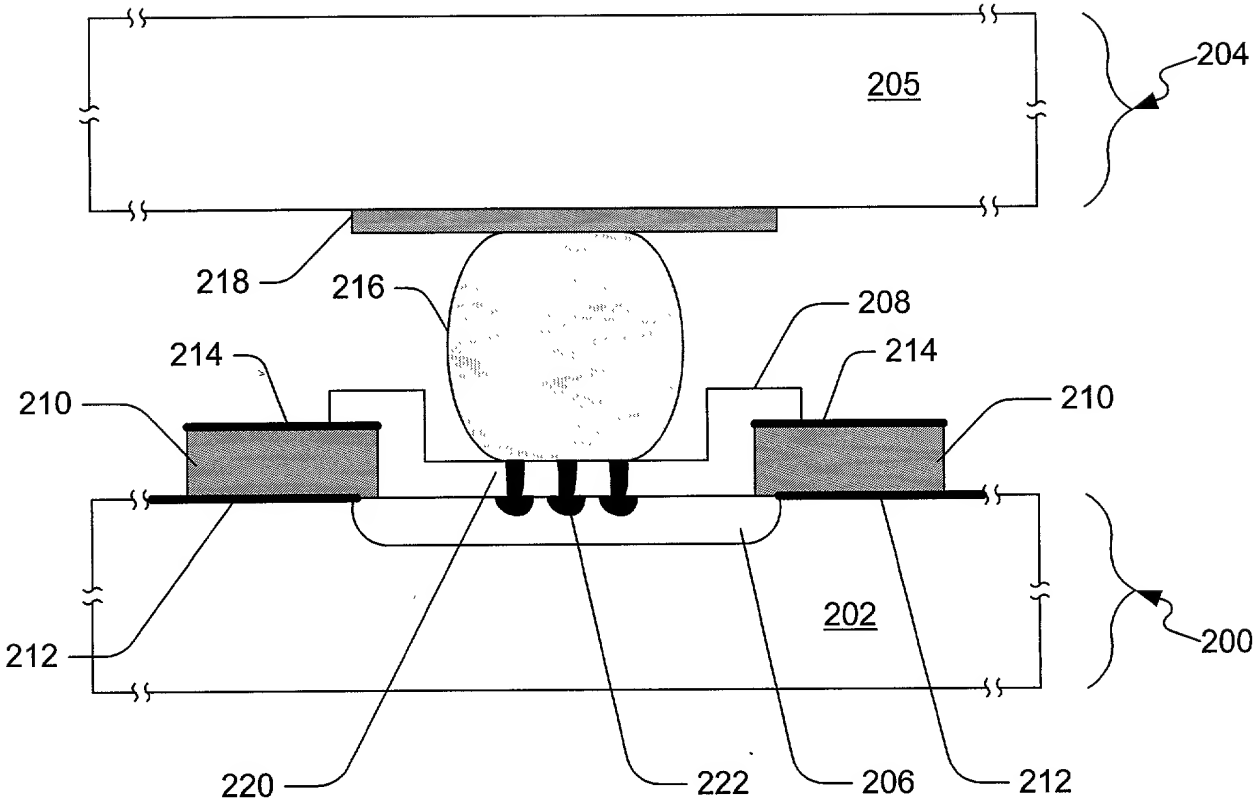

FIG. 2
(PRIOR ART)

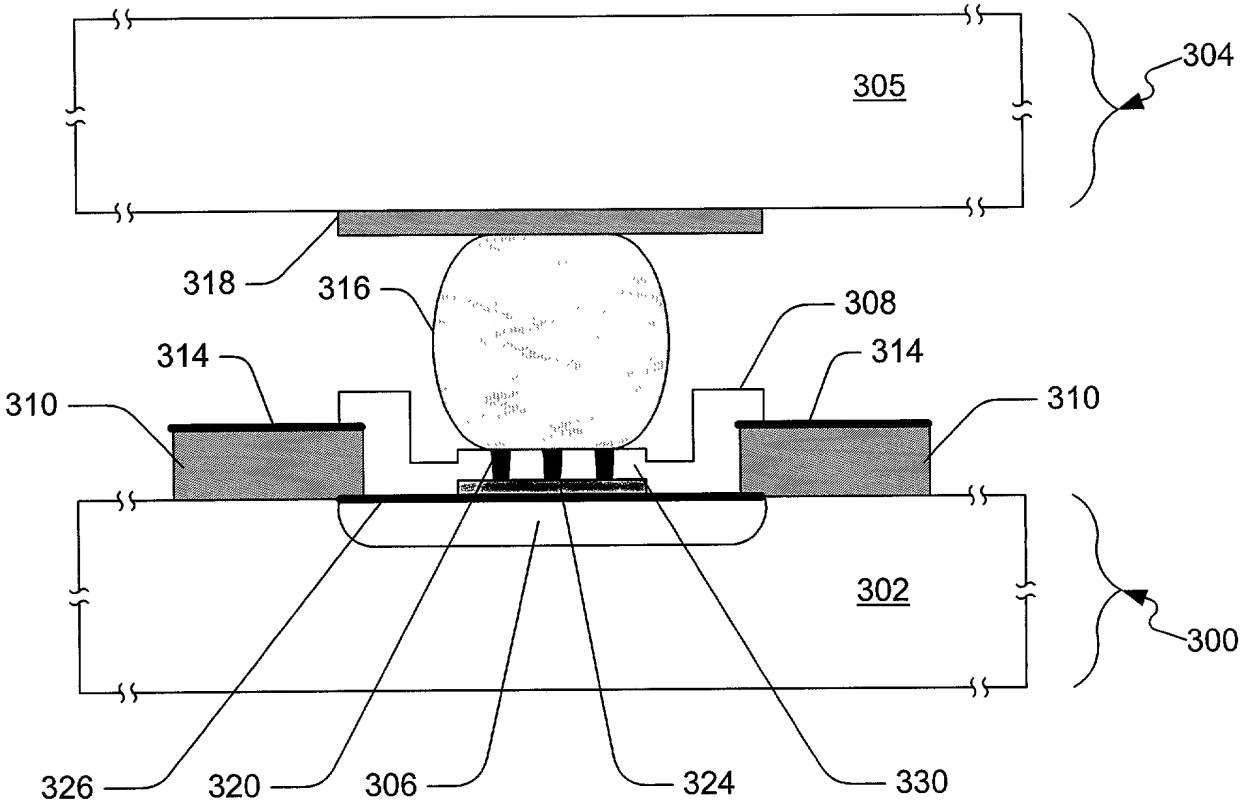

FIG. 3

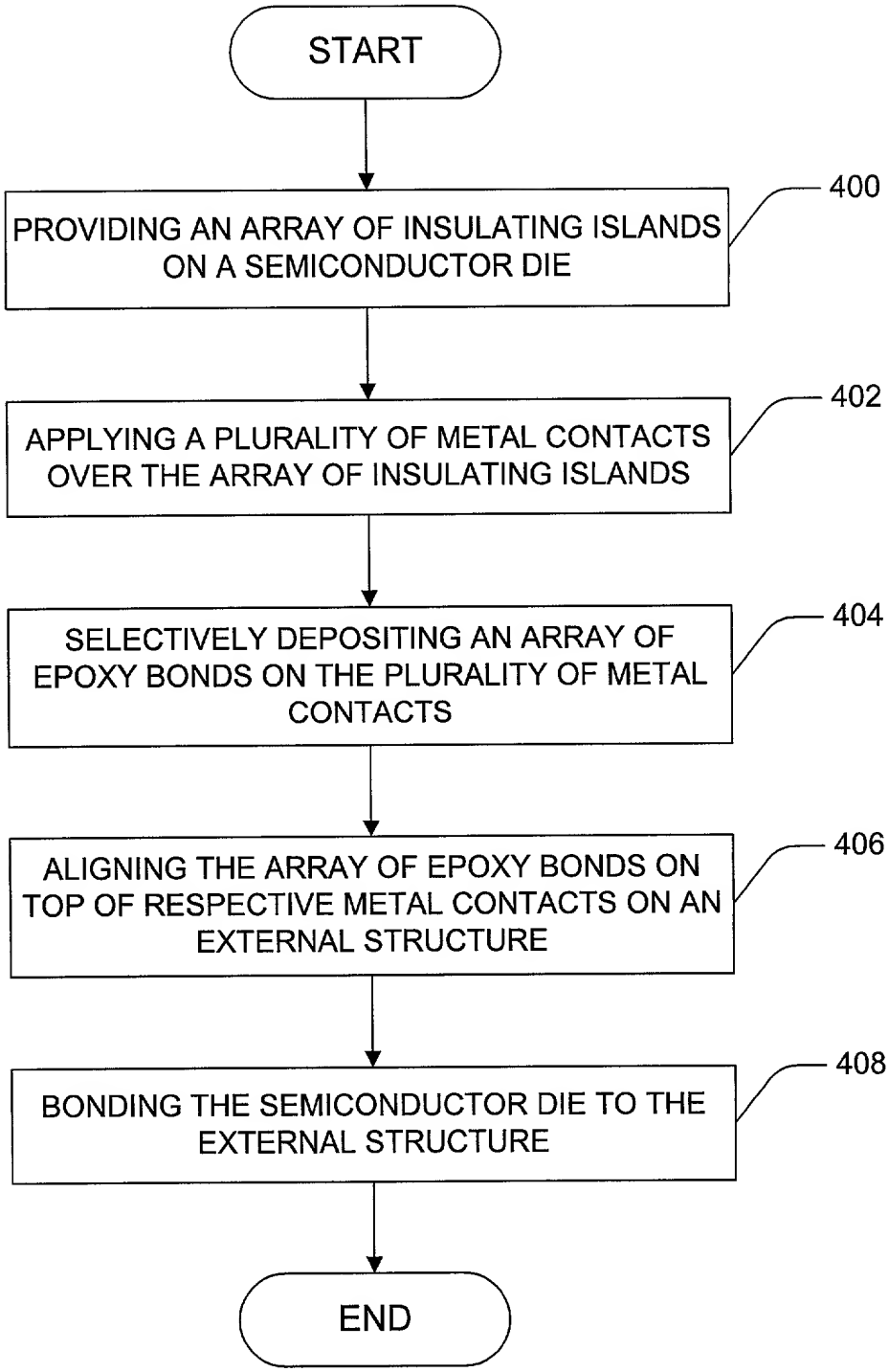
START
PROVIDING AN ARRAY OF INSULATING ISLANDS ON A SEMICONDUCTOR DIE
400
APPLYING A PLURALITY OF METAL CONTACTS OVER THE ARRAY OF INSULATING ISLANDS
402
SELECTIVELY DEPOSITING AN ARRAY OF EPOXY BONDS ON THE PLURALITY OF METAL CONTACTS
404
ALIGNING THE ARRAY OF EPOXY BONDS ON TOP OF RESPECTIVE METAL CONTACTS ON AN EXTERNAL STRUCTURE
406
BONDING THE SEMICONDUCTOR DIE TO THE EXTERNAL STRUCTURE
408
END

FIG. 4

Attorney's Docket No.: 07402-039001

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled INSULATOR/METAL BONDING ISLAND FOR ACTIVE AREA SILVER EPOXY BONDING, the specification of which:

[X] is attached hereto.
[] was filed on ____ as Application Serial No. _ and was amended on _____.
[] was described and claimed in PCT International Application No. _____ filed on _____ and as amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information I know to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim the benefit under Title 35, United States Code, §119(e)(1) of any United States provisional application(s) listed below:

U.S. Serial No.	Filing Date	Status
60/128,626	4/9/99	Pending

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose all information I know to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

U.S. Serial No.	Filing Date	Status

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Country	Application No.	Filing Date	Priority Claimed

I hereby appoint the following attorneys and/or agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: John B. Pegram, Reg. No. 25,198; Stephan J. Filipek, Reg. No. 33,384; Richard J. Anderson, Reg. No. 36,732; Ingrid Beattie, Reg. No. 42,306; Robert M. Bedgood, Reg. No. 43,488; Mark S. Ellinger, Reg. No. 34,812; J. Eldora L. Ellison, Reg. No. 39, 967; Peter Fasse,

Attorney's Docket No.: 07402-039001

Combined Declaration and Power of Attorney

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Address all correspondence to SAMUEL S. LEE at:

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San Diego, CA 92122

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

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Inventor's Signature: _____ Date: April 7 2000
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Encinitas, California 92007